University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

Roll No. - [redacted]

THEORY EXAMINATION – DEC 2022	
B.TECH - ECE	SEMESTER – III

TIME – 3 Hrs.

M.M. - 75

PAPER - EC-205

SUBJECT- Digital Electronics

Note: All questions in Part-A and Part-B are compulsory. Attempt any four questions from Part-C selecting at least one from each unit.

PART-A (15 Marks)

Q. No. – 1 Answer the following questions. **15x1=15**

(i)	Describe BCD codes. Convert $(79)_{10}$ to binary, excess 3 and BCD codes.
(ii)	State De-Morgan's theorem,
(iii)	Construct hamming code for BCD 0110. Use even parity.
(iv)	List the characteristics (at least 8) of digital ICs.
(v)	Draw and explain conversion method used in Binary to Grey code convertor.
(vi)	Discuss the function of 2-bit comparator. Draw truth table for a 2-bit comparator.
(vii)	Draw a labelled block diagram of n:1 MUX. Mention significance of enable pin in multiplexer.
(viii)	Implement the expression using a suitable multiplexer: $f(A,B,C,D)= \sum m(0,1,3,5,6,7,9,13,14)$
(ix)	Mention difference between sequential circuits and combinational circuits.
(x)	Differentiate between Latch and flip flop.
(xi)	Draw the timing diagram of output waveform of serial in- serial out register for binary input 011001 using falling edge triggering.
(xii)	Define state diagram and state table.
(xiii)	Draw a basic sample and hold circuit. Describe its working.
(xiv)	Differentiate between PAL and PLA.
(xv)	Draw timing diagram for read and write cycle in memory.

PART-B (20 Marks)

	UNIT-I	
2	a) Explain how universal gates can be used as AND and OR gates. b) **Discuss use of Hamming codes as error correcting codes.**	5
	UNIT-II	
3	**Construct a 16:1 MUX using two 8:1 Mux and a 2:1 Mux. Explain its working.**	5
	UNIT-III	
4	**Interpret race around condition of J-K flipflop. Explain how is it removed in master-slave flip flop.**	5
	UNIT-IV	
5	**Draw and explain working of weighted register DAC.**	5

PART-C (40 Marks)

	UNIT-I	
6	a) **Perform the following operations: i) -48 -23 using 2's complement ii) 45-15 using 1's Complement method.** b) **Simplify the given function using K-map: F(A,B,C,D)= $\sum$ m(1,3,5,7,8,10) + d(9,11,13). Realize the obtained minimized expression using AOI logic.**	4 6
7	a) **Prove the following using Boolean algebraic theorems: i)** $A.B + \bar{A}.B + A.\bar{B} = \bar{A} + B$ **ii)** $(A + B).(C + D) = \overline{(\overline{A + B}) + (\overline{C + D})}$ b) **Draw logic circuit of three input TTL NAND gate. Explain its working. Mention the significance of Totem Pole output.**	4 6
	UNIT-II	
8	**Design a four-bit BCD adder. Explain its working. Mention why a 0110 needs to be added in order to obtain correct output.**	10
9	**Design an octal to binary priority encoder.** **Design a parity generator circuit to add an odd parity bit to a 7 bit word.**	5 5
	UNIT-III	
10	**Design a 3 bit up-down synchronous counter. Use J-K flip flop for counter designing.**	10
11	**What are registers? Explain application of shift register as ring counter. Draw the output w for the circuit.** **Design a serial in- parallel out shift right register.**	5 5
	UNIT-IV	
12	**What is RAM? Draw basic bipolar RAM cell. Describe its working.** **Write note on different types of memories.**	5 5
13	**List the specifications of DAC. Explain them in detail.** **Explain how a dual slope ADC works?**	5 5