University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

THEORY EXAMINATION – JULY 2021	
B.TECH - ECE	**SEMESTER – VI**

TIME – 4 Hrs.

M.M. - 75

PAPER - EC-306

SUBECT - VERILOG HDL

INSTRUCTIONS TO BE FOLLOWED

- **The candidates will be required to attempt All questions in Part-A and Part-B (Compulsory Sections). Attempt any four questions from Part-C selecting at least one from each unit.**
- **Allotted time for examination is 4 hours that includes time for downloading the question paper, writing answers, scanning of answer sheets and uploading the sheets on the Attendance Sheet Cum Answer Sheet Uploading google form. The link will be closed after the stipulated time.**
- **The PDF files should be saved as Roll No. and Subject Code.**
- **Maximum Page Limit should be 36 (Thirty Six) for attempting the question paper on A4 sheets which could be downloaded and printed from the sample sheets given in the UIET Website.**
- **Over-attemptation should be avoided.**
- **Handwriting should be neat and clean and diagrams should be clear and contrasted.**
- **The candidate should not write their Mobile No. otherwise Unfair Means Case will be made.**
- **While attempting the paper, the candidate will use blue/black pen only.**
- **Before attempting the paper, the candidate will ensure that he/she has downloaded the correct question paper. No complaint for attempting wrong question paper by the candidate will be entertained.**
- **Candidate must ensure that he/she has put his/her signature on each page of the answer sheet used by him/her. Answer sheet without the signature of the candidate will not be evaluated.**
- **Attempt parts A, B & C separately. Do not inter-mix them. Write neatly & mention the question number clearly.**

PART-A (15 Marks)

Q. No. – 1 Answer the following questions. 15x1=15

(i)	The default value for reg data type is _____..
(ii)	Write the syntax for NOR gate primitive.
(iii)	Write functional description of bufif1.
(iv)	Explain the statement #100 $stop.
(v)	Strength for strong 0 is……...
(vi)	To suspend a simulation, you can use this system task command.
(vii)	If A= 4'b1011 write A>2
(viii)	@posedge means
(ix)	Define keyword deassign.
(x)	_____ defines special parameters in the specify block. a) Specparam b) defparam c) param d) parameter
(xi)	Explain trireg net.
(xii)	..... declaration is not supported by UDP
(xiii)	Explain reduction XNOR.
(xiv)	Write the syntax for CMOS switch.
(xv)	Explain pullup.

PART-B (20 Marks)

	UNIT-I	
2	**Explain scalars and vectors with example.**	**5**
	UNIT-II	
3	**Describe contention with example.**	**5**
	UNIT-III	
4	**Explain logical and relational operators with example.**	**5**
	UNIT-IV	
5	**Differentiate between blocking and non- blocking assignment statements.**	**5**

PART-C (40 Marks)

	UNIT-I	
6	**Explain ASIC design and development flow.**	**10**
7	**Explain test bench.** **Explain synthesis and simulation.**	**5,5**
	UNIT-II	
8	**Realize and design Master slave J- flip flop using gate level modelling.**	**10**
9	**Explain case construct and write a program for 2:4 decoder using behavioural modelling.**	**4,6**

UNIT-III		
10(a)	**Explain different types of delays.**	**5**
(b)	**Explain and design 8-bit adder using dataflow modelling.**	**5**
11(a)	**Explain resistive switches.**	**4**
(b)	**Explain working of 2 input AND gate using active pull up load and also write a program for it.**	**6**
UNIT-IV		
12	**Define half adder and full adder as tasks and prepare a 32-bit adder using them. Also write test bench for it.**	**4,6**
13	**Explain the following terms.** **1) Compiler directives** **2) Module paths**	**10**