QUESTION PAPER CODE- 54022

University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

Roll No. -

THEORY EXAMINATION – MAY 2019	
B.TECH -ECE	SEMESTER – 4th

TIME – 3 Hrs.

M.M. - 75

PAPER- ECE-210

SUBJECT–Computer Architecture and Organization

Note: All questions in Part-A and Part-B are compulsory. Attempt any four questions from Part-C selecting at least one from each unit.

PART-A (15 Marks)

Q. No. – 1 Answer the following questions. **15x1=15**

(i)	What is selective set and selective compliment logical micro-operations? Explain with the help of examples.
(ii)	What are single address and zero address instructions? Explain.
(iii)	What is a stack? Describe the format of PUSH and POP instructions present in a stack.
(iv)	Differentiate between RISC and CISC instructions.
(v)	Which are the two techniques of creating 9's compliment in BCD subtractor? Explain with the help of an example.
(vi)	What is multiprocessing? Give any example.
(vii)	What is memory hierarchy? Draw its diagram.
(viii)	What is memory management hardware?
(ix)	Draw the 1D-RAM cell and also explain its working.
(x)	What is an auxillary memory? Give examples. Why it is used.
(xi)	What is a pipeline? Draw its basic structure with the help of an example.
(xii)	Explain memory interleaving with the help of a diagram.
(xiii)	What is an interface unit? Why it is used?
(xiv)	What is an Associative memory? Explain.
(xv)	What is Simplex, Half duplex and Full duplex communication.

PART-B (20 Marks)

	UNIT-I	
2	(a) Draw and explain the Von-Neumann architecture of a basic computer system. (b) What are Macros and Subroutines? Explain in detail with the help of diagrams.	2.5 2.5
	UNIT-II	
3	(a) What are Array processors? On which classification structure Array processors are based? Explain. (b) Describe the working of a Crossbar switch.	2.5 2.5
	UNIT-III	
4	(a) Differentiate between SRAM and DRAM semiconductor memories. (b) What is a cache memory? Explain its working.	2.5 2.5
	UNIT-IV	
5	(a) If the number of tasks in a pipeline are 7 and segments are 5. Determine the number of clock cycles needed to complete the task. Also draw the space-time diagram for the same. (b) Discuss the complete process of communication between IOP and a CPU	2.5 2.5

PART-C (40 Marks)

	UNIT-I	
6	(a) What is register transfer? Explain the process of register transfer with the help of a timing Diagram. (b) Discuss the arithmetic micro-operations. Also specify, how the working of a binary adder differs from the working of a binary adder-subtractor.	5 5
7	What are addressing modes? Why they are used? Specify the prominent addressing modes. Find the operand using (i) Register direct (ii) Register indirect (iii) Relative mode (iv) Auto increment (v) Auto decrement. Two word instruction is load to Accumulator and address field is 500. Initial Value of program counter (PC) is 200 and general register (R1) is 400.	10

Address	Memory
200	Load to Accumulator
201	Address=500
202	Next instruction
399	450
400	700
401	800
702	325

	UNIT-II	
8	(a) What are the differences between a micro-programmed control and hardwired control design units. (b) Describe the working of a Multiplier control unit with the help of a block diagram.	5 5
9	(a) What are the different decimal arithmetic operations? Explain the three techniques to perform addition of decimal numbers. (b) Explain the parallel processing based on Flynn's classification structures.	5 5
	UNIT-III	
10	The size of each RAM chip is 128x8 and ROM chip is 512x8. If a computer system needs 512 bytes of RAM and 512 bytes of ROM. Draw the memory address map for thegiven capacity of a computer system. Also, draw a diagram for memory connection to CPU.	10
11	What is an address space and a memory space? Explain the complete process of mapping from a virtual address to a main memory address by taking any example of your choice.	10
	UNIT-IV	
12	(a) What is a RISC pipeline? Explain the process of Delayed load and Delayed branch by taking any example of your choice. (b) What is vector processing? Explain the process of Matrix multiplication by using a multiplier and adder pipeline segments for the calculation of an inner product.	5 5
13	(a)Discuss strobe control and handshaking process in Asynchronous data transfer. (b) Discuss in brief DMA controller and DMA transfer.	5 5