University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

TIME – 3 Hrs 15 Min

THEORY EXAMINATION –JAN 2021	
B.TECH - ECE	**SEMESTER - V**

M.M. - 56

PAPER - ECP-5	**SUBJECT- VLSI TECHNOLOGY**

INSTRUCTIONS TO BE FOLLOWED

- **Allotted time for examination is 3 hours 15 minutes that includes time for downloading the question paper, writing answers, scanning of answer sheets and E-mailing the PDF files to the designated Email ID.**
- **For ECE-A Regular Students, the Email ID is:- btech5thecea@kuk.ac.in**
- **For ECE-B Regular Students, the Email ID is:- btech5theceb@kuk.ac.in**
- **The candidates will be required to attempt 75% of the question paper (maximum) by choosing to their any best questions accumulating 56 marks.**
- **The PDF files should be saved as Roll No. and Subject Code. Proper attention should be given while sending the email and in the subject line, the Roll Number and Subject Code should be mentioned.**
- **Maximum Page Limit should be 20 (Twenty) for attempting the question paper on A4 sheets which could be downloaded and printed from the sample sheets given in the Kurukshetra University Examination guidelines.**
- **Over-attemptation should be avoided.**
- **Handwriting should be neat and clean and diagrams should be clear and contrasted.**
- **The candidate should not write their Mobile No. otherwise Unfair Means Case will be made.**
- **While attempting the paper, the candidate will use blue/black pen only.**
- **Before attempting the paper, the candidate will ensure that he/she has downloaded the correct question paper. No complaint for attempting wrong question paper by the candidate will be entertained.**
- **Candidate must ensure that he/she has put his/her signature on each page of the answer sheet used by him/her. Answer sheet without the signature of the candidate will not be evaluated.**

PART-A

Q. No. – 1 Answer the following questions. 15x1=15

(i)	Define monolithic IC. How it is different from hybrid IC ?
(ii)	List the technique used for Si crystal growth.
(iii)	Explain how wafer defects can be removed?
(iv)	Discuss how various parameters of the Si crystal are measured?
(v)	Explain the need of epitaxy?
(vi)	Explain the need of Oxidation?
(vii)	Define channelling in ion implantation?
(viii)	Define lithography.
(ix)	Explain briefly various types of lithography.
(x)	Explain the use of etching in VLSI ?
(xi)	Differentiate between dry and wet etching.
(xii)	Explain the use of packaging.
(xiii)	Explain the need of metallization technique.
(xiv)	Define Yield in VLSI.
(xv)	Define Reliability in VLSI.

PART-B

2	Explain briefly the theory of growth of Oxide layer on Si substrate.	5
3	Explain briefly Molecular Beam Epitaxy process.	5
4	Differentiate between positive and negative photoresists with examples.	5
5	Explain various fabrication steps of NMOS IC.	5

PART-C

6	Explain the Czochralski technique of Silicon crystal growth with all the necessary diagrams And equations.	10
7	Explain in detail the plasma oxidation. What are the various defects induced by oxidation.	10
8	Explain Growth kinetics of epitaxial layer deposition. What is the apparatus required for Silicon epitaxial process.	10
9	Explain Diffusion with Diffusion models of solid. Describe Fick's theory of diffusion with Solution of Fick`s law.	10
10	Differentiate between Optical and non-optical lithography process with necessary diagrams.	10
11	Explain X-ray lithography and ion-beam lithography techniques with necessary diagrams.	10
12	Explain various fabrication steps of PMOS IC with necessary diagrams.	10
13	Explain Packaging, its types , packaging design consideration along with VLSI assembly technologies	10