University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

THEORY EXAMINATION – JAN 2021	
B.TECH - ECE	**SEMESTER – V**

TIME – 3 Hrs 15 Min

M.M. - 56

PAPER - EC-305

SUBJECT- Computer Architecture & Organization

INSTRUCTIONS TO BE FOLLOWED

- **Allotted time for examination is 3 hours 15 minutes that includes time for downloading the question paper, writing answers, scanning of answer sheets and E-mailing the PDF files to the designated Email ID.**
- **For ECE-A Regular Students, the Email ID is:- btech5thecea@kuk.ac.in**
- **For ECE-B Regular Students, the Email ID is:- btech5theceb@kuk.ac.in**
- **The candidates will be required to attempt 75% of the question paper (maximum) by choosing to their any best questions accumulating 56 marks.**
- **The PDF files should be saved as Roll No. and Subject Code. Proper attention should be given while sending the email and in the subject line, the Roll Number and Subject Code should be mentioned.**
- **Maximum Page Limit should be 20 (Twenty) for attempting the question paper on A4 sheets which could be downloaded and printed from the sample sheets given in the Kurukshetra University Examination guidelines.**
- **Over-attemptation should be avoided.**
- **Handwriting should be neat and clean and diagrams should be clear and contrasted.**
- **The candidate should not write their Mobile No. otherwise Unfair Means Case will be made.**
- **While attempting the paper, the candidate will use blue/black pen only.**
- **Before attempting the paper, the candidate will ensure that he/she has downloaded the correct question paper. No complaint for attempting wrong question paper by the candidate will be entertained.**
- **Candidate must ensure that he/she has put his/her signature on each page of the answer sheet used by him/her. Answer sheet without the signature of the candidate will not be evaluated.**

PART-A

Q. No. – 1 Answer the following questions. 15x1=15

(i)	Differentiate between memory stack and memory stack.
(ii)	What are one address and zero address instructions? Give examples.
(iii)	Differentiate between Macro and Subroutine instructions.
(iv)	Why is RISC preferred over CISC instructions?
(v)	Discuss the architecture of time shared common bus.
(vi)	What are the types of micro controlled signals?
(vii)	Draw the diagram of attached array processor.
(viii)	What is multiprocessing?
(ix)	Differentiate between SRAM and DRAM.
(x)	What are peripheral devices?
(xi)	What is an IOP?
(xii)	What is FIFO and LIFO?
(xiii)	Differentiate between random access memory and serial access memory.
(xiv)	List two characteristics of memory devices.
(xv)	List some applications of multiprocessing.

PART-B

2	Draw and explain the Von Neumann architecture of Computer architecture.	5
3	Discuss the operation of BCD adder.	5
4	What is Cache memory? Discuss the case of direct mapping in case of virtual memory.	5
5	Discuss in brief the case of Delayed load and Delayed branch.	5

PART-C

6	What are addressing modes? Why they are used? Specify the prominent addressing modes. Find the operand using (i) Register direct (ii) Register indirect (iii) Relative mode (iv) Auto increment (v) Auto decrement. Two word instruction is load to Accumulator and address field is 500. Initial Value of program counter (PC) is 200 and general register (R1) is 400.	**10**

Address	Memory
200	Load to Accumulator
201	Address=500
202	Next instruction
399	450
400	700
401	800
702	325

7	What is a micro-operation? Explain with the help of an example. Define Register transfer language. Draw and explain the timing diagram to show the transfer among two registers**.**	**10**
8	(a) Differentiate between hardwired control and micro programmed control. (b) Discuss address sequencing in micro programmed control.	**10**

9	What is parallel processing? Why it is used? List some advantages of parallel processing. Explain SIMD and MIMD structures of parallel processing.	**10**
10	What is an address space and a memory space? Explain the complete process of mapping from a virtual address to a main memory address by taking any example of your choice.	**10**
11	The size of the memory to be constructed is 1024 x 8 with 128 x 8 RAM chips and 512 x 8 ROM chips. If the Size of each RAM chip is 128 x 8 and size of ROM chip is 512 x 8. Then, How many RAM and ROM chips have to be used? Draw the memory address map table and Connection diagram to the CPU for the same.	**10**
12	Discuss the following: (a) DMA controller and DMA transfer (b) Asynchronous data transfer	**10**
13	What is pipelining? Discuss in detail the process of arithmetic pipeline.	**10**