***University Institute of Engineering & Technology***

*(Recognised Under Section 2(f) and 12B of UGC)*

***Kurukshetra University, Kurukshetra***

**TIME – 3 Hrs 15 Min**

| **THEORY EXAMINATION – FEB 2021** | |
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| **B.TECH - ECE** | **SEMESTER - III** |

**M.M. - 56**

**PAPER - EC-205**

**SUBJECT- DIGITAL ELECTRONICS**

## INSTRUCTIONS TO BE FOLLOWED

- **Allotted time for examination is 3 hours 15 min that includes time for downloading the question paper, writing answers, scanning of answer sheets and E-mailing the PDF files to the designated Email ID.**
- **All the ECE-A students should send their answer sheets on this Email ID- btech3rdecea@kuk.ac.in**
- **All the ECE-B regular and reappear students should send their answer sheets on this Email ID- btech3rdeceb@kuk.ac.in**
- **The candidates will be required to attempt 75% of the question paper (maximum) by choosing to their any best questions accumulating 56 marks.**
- **The PDF files should be saved as Roll No. and Subject Code. Proper attention should be given while sending the email and in the subject line, the Roll Number and Subject Code should be mentioned.**
- **Maximum Page Limit should be 20 (Twenty) for attempting the question paper on A4 sheets which could be downloaded and printed from the sample sheets given in the Kurukshetra University Examination guidelines.**
- **Over-attemptation should be avoided.**
- **Handwriting should be neat and clean and diagrams should be clear and contrasted.**
- **The candidate should not write their Mobile No. otherwise Unfair Means Case will be made.**
- **While attempting the paper, the candidate will use blue/black pen only.**
- **Before attempting the paper, the candidate will ensure that he/she has downloaded the correct question paper. No complaint for attempting wrong question paper by the candidate will be entertained.**
- **Candidate must ensure that he/she has put his/her signature on each page of the answer sheet used by him/her. Answer sheet without the signature of the candidate will not be evaluated.**

## PART-A

**Q. No. – 1 Answer the following questions. 15x1=15**

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|---|---|
| **(i)** | **Convert $378.93_{10}$ to octal..** |
| **(ii)** | **Express -45 in 8 bit 2's complement form.** |
| **(iii)** | **Substract $78D6.3B_{16}$ from $B08E.A1_{16}$.** |
| **(iv)** | **Define the term fan out?** |
| **(v)** | **State Associative law.** |
| **(vi)** | **Write Down differences between Demultiplexer and decoder.** |
| **(vii)** | **Give two examples of sequential circuits.** |
| **(viii)** | **Suggest a solution to overcome the limitation on the speed of an adder.** |
| **(ix)** | **Mention two differences between the edge triggering &level triggering.** |
| **(x)** | **Write the characteristic equation of a SR flip flop.** |
| **(xi)** | **Convert JK flip flop to D flip flop.** |
| **(xii)** | **A 4 bit binary ripple counter is operated with clock frequency of 1khz. What is the output frequency of its third flip flop.** |
| **(xiii)** | **List various type of A/D converters.** |
| **(xiv)** | **What is the difference between PAL & PLA?** |
| **(xv)** | **What s volatile and Non volatile memory.** |

## PART B

| | | |
|---|---|---|
| **2** | **Prove that an AND-OR configuration is equivalent to a NAND-NAND configuration.** | **5** |
| **3** | **Implement a full substractor circuit using minimum number of NAND gates only.** | **5** |
| **4** | **Draw the logic diagram and timing diagram of a 3 bit binary ripple up counter using positive edge triggered FFs.** | **5** |
| **5** | **What is RAM and ROM. What is the basic difference between EPROM and EEROM.** | **5** |

## PART-C

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|---|---|---|
| **6** | **(a) Substract 27.50 from 68.75 using the 12-bit 1's complement arithmetic.**<br>**(b) Perform subtraction of 147.8 from 206.7 using 8421 BCD code.**<br>**(c) Perform addition of 247.6 and 359.4 using XS-3 code.** | **(4)**<br>**(3)**<br>**(3)** |

| | | |
|---|---|---|
| **7** | **Obtain the minimal SOP expression for Σm(0,2,3,10,12,16,17,18,21,26,27) & implement it in NOR logic.** | **10** |
| **8** | **What is look-ahead carry adder? Discuss the circuit and working of look-ahead carry adder.** | **10** |
| **9** | **What is a comparator. Discuss the circuit & working of a 2 bit comparator.** | **10** |
| **10** | **Explain the operation of a 4 bit bidirectional shift register with the help of a circuit diagram.** | **10** |
| **11** | **(a) Draw the circuit of an S-R flipflop using NAND gates. Modify it to include clock. Derive J-K circuit from S-R flipflop circuit & explain its,truth table.**<br>**(b) Write down the differences between combinational logic circuits and sequential logic Circuits.** | **7**<br>**3** |
| **12** | **(a) Describe the working principle of R-2R ladder D/A converter.**<br>**(b) Describe parallel comparator ADC with suitable diagram.** | **5**<br>**5** |
| **13** | **What is PLA ? What are its application ? Discuss the design &working of a PLA.** | **10** |