University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

TIME – 3 Hrs 15 Min

THEORY EXAMINATION – JAN 2021	
B.TECH - CSE	**SEMESTER - V**

M.M. - 56

PAPER - ES-301

SUBJECT- Microprocessor & Interfacing

INSTRUCTIONS TO BE FOLLOWED

- **Allotted time for examination is 3 hours 15 minutes that includes time for downloading the question paper, writing answers, scanning of answer sheets and E-mailing the PDF files to the designated Email ID.**
- **For CSE-A Regular Students, the Email ID is:- btech5thcsea@kuk.ac.in**
- **For CSE-B Regular Students, the Email ID is:- btech5thcseb@kuk.ac.in**
- **The candidates will be required to attempt 75% of the question paper (maximum) by choosing to their any best questions accumulating 56 marks.**
- **The PDF files should be saved as Roll No. and Subject Code. Proper attention should be given while sending the email and in the subject line, the Roll Number and Subject Code should be mentioned.**
- **Maximum Page Limit should be 20 (Twenty) for attempting the question paper on A4 sheets which could be downloaded and printed from the sample sheets given in the Kurukshetra University Examination guidelines.**
- **Over-attemptation should be avoided.**
- **Handwriting should be neat and clean and diagrams should be clear and contrasted.**
- **The candidate should not write their Mobile No. otherwise Unfair Means Case will be made.**
- **While attempting the paper, the candidate will use blue/black pen only.**
- **Before attempting the paper, the candidate will ensure that he/she has downloaded the correct question paper. No complaint for attempting wrong question paper by the candidate will be entertained.**
- **Candidate must ensure that he/she has put his/her signature on each page of the answer sheet used by him/her. Answer sheet without the signature of the candidate will not be evaluated.**

PART-A

Q. No. – 1 Answer the following questions. 15x1=15

(i)	What are the functions of BIU and EU in 8086 processor?
(ii)	Explain the concept of memory segmentation in 8086 microprocessor?
(iii)	Give the PSW format of 8086?
(iv)	What is queue? How queue is implemented in 8086?
(v)	In 8086 processor the code segment contains 6000H and instruction pointer contains 9F20H. Find the memory location addressed by the processor.
(vi)	Explain detail about the addressing modes of 8086?
(vii)	What is assembler Directives? Explain 4 assembler directives in detail?
(viii)	What is the RESET vector of 8086?
(ix)	What does the RET statement cause to happen?
(x)	When multi-byte BCD numbers are added, which is the instruction to be used to correct the result?
(xi)	When two numbers are added, the sum is 08, and it is in BL. What is the instruction to be used to convert this number to ASCII form?
(xii)	When connecting a 2K ROM to the 8086, how many address lines of the processor can be used for address decoding?
(xiii)	Which signal is generated by the 8086 to access the odd bank of memory?
(xiv)	In variable port addressing, the address of the I/O port is loaded into which 8086 register?
(xv)	INTR is not a vectored interrupt .What does this statement mean?

PART-B

2	A device which is 2 times slower than the 8086 µp has to be interfaced with 8086.With the help of a circuit diagram generate show how many wait states are to be introduced in 8086 µp and where will the wait states be inserted in the T-states?	**5**
3	Draw and discuss the write cycle timing diagram of 8086 in minimum mode?	**5**
4	Gnerate the HEX codes for the following instructions i. Mov [BP+SI], 3987h ii. Mov Ax, [CX]	**5**
5	Write down the steps involved when an interrupt INT 32h is encountered in the main program and calculate address of ISR for this interrupt?	**5**

PART-C

6	Draw the relevant pin diagram for 8086 Microprocessor and explain function of each pin in detail?	**10**
7	Draw the Internal architecture of 8086 microprocessor & explain the concept of memory banks in 8086 microprocessor?	**10**
8	Interface the 8086 microprocessor with two 16Kx16 EPROM chips and two 16Kx16 RAM chips. Draw the necessary block diagram for the support of your calculations?	**10**

9	Draw and explain the timing diagram for RD operation from an I/O device in MX Mode of 8086?	**10**
10	Explain the following instructions:- 1. LDS 2.XLAT 3. AAA 4. DAA 5. ROL Write an ALP in 8086 to add two 16-digit packed BCD numbers?	**10**
11	(a) Calculate the memory address the following instructions will access If DS = 4000H, [BX] = 0100H, and [SI] = 6000H, [BP] = 1000H and [DI] = 2100H. Also explain the addressing modes that are used by each instruction. a. MOV CX, [1234H] b. MOV AX, [2222H] c. MOV DX, [BX] d. MOV DX, [BP+DI] e. MOV DX, [BX + SI + 200H] f. MOV DX, [BP + DI + 01H] g. MOV AX, 1234H **(b)** Explain AAA, TEST, LEA, instructions with examples.	**10**
12	Interface 8-bit ADC with 8086 using 8255 ports. Configure port A of 8255 for transferring output of ADC to the CPU and port C for control signals. Assume that an analog input is present at I/P6 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write the required assembly language program?	**10**
13	Interface a typical 12-bit DAC with 8255 and write a program to generate a triangular waveform of period 10 ms. The CPU runs at 6 MHz clock frequency.	**10**