## **QUESTION PAPER CODE-51044**

## University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

## Kurukshetra University, Kurukshetra

Roll No. - 2 5/6-1/25

THEORY EXAMINATION - DEC 2019

B.TECH - ECE SEMESTER - III

TIME - 3 Hrs.

M.M. - 75

PAPER- EC-205

SUBJECT - DIGITAL ELECTRONICS

Note: All questions in Part-A and Part-B are compulsory. Attempt any four questions from Part-C selecting at least one from each unit.

PART-A (15 Marks)

|        | -1 Answer the following questions.  | 15x1=15  |
|--------|---|--|
| 7      | Convert 01011111011.01111112 to hexadecimal.  |  |
| 7      | Express -73.75 in 12 bit 2's complement form.   |  |
| iy .   | Apply De-Morgan's Theorem to $\overline{((A+B)+C)}$   | ].   |
| ) 1    | Define the term fan out?  |  |
| 7 s    | State Distributive law.   |  |
| V      | Vrite Down differences between Demultiplexer  | r and decoder.   |
| ) G    | live four examples of combinational circuits.   |  |
| 1      | uggest a solution to overcome the limitation on<br>ention two differences between the edge trigge         |  |
|        | rite the characteristic equation of a JK flip flo   | 1,   |
| Co     | onvert JK flip flop to T flip flop.   | 10 (10 to 10 |
| A 4    | bit binary ripple counter is operated with clo  | ock frequency of 1khz. What is the output frequency o  |
| 1:.    | third flip flop.  | The output fragues and is the output fragues and   |
| its Wh | at is propagation delay.  | output frequency o   |
| Wh     | at is propagation delay.  | where we have the director of  |
| Wh     | at is propagation delay.  at is the difference between PAL & PLA?  at s volatile and Non volatile memory. | Answers and the second  |

|   | UNIT-I   |   |
|---|--|---|
| 2 | What is the importance and applications of Gray codes? Convert binary number 10100111 to gray code.              | 5 |
|   | UNIT-II  |   |
| 3 | Implement a full adder circuit using minimum number of NAND gates only.  | 5 |
|   | UNIT-III   |   |
| 4 | Draw the logic diagram and timing diagram of a 3 bit binary ripple up counter using positive edge triggered FFs. | 5 |
| - | TINITO IN  |   |
| 5 | What are the various types of ROM's? Discuss their relative advantages and disadvantages.                        | 5 |

## PART-C (40 Marks)

|     | UNIT-I  |                   |
|-----|---|-------------------|
| 6   | <ul> <li>(a) Add -31.5 to -93.125 using the 12-bit 2's complement arithmetic.</li> <li>(b) Perform subtraction of 27.8 from 57.6 using xs-3 arithmetic.</li> <li>(c) Design all the gates using only NAND gates.</li> </ul> | (4)<br>(3)<br>(3) |
| T)  | Obtain the minimal SOP expression for $\Sigma m(0,1,2,3,5,7,8,9,10,12,13)$ & implement it in NAND logic.  | 10                |
|     | UNIT-II   | 1                 |
| 8   | What is seven segment display? Discuss the circuit and working of a seven segment decoder.  | 10                |
| 9   | What is a comparator. Discuss the circuit & working of a 2 bit comparator.  | 10                |
| •   | UNIT-III  |                   |
| 10  | Explain the operation of a 4 bit bidirectional shift register with the help of a circuit diagram.   | 10                |
|     |   |                   |
| 11/ | <ul> <li>(a) Draw the circuit of Master/slave JK flip flop and explain the operation of the circuit.</li> <li>(b) What do you mean by o's catching and i's catching phenomena in master/slave JK Flip Flop.</li> </ul>      | 7 3               |
| 11/ | (b) What do you mean by o's catching and i's catching phenomena in master/slave   | 1.                |
| 11/ | (b) What do you mean by o's catching and i's catching phenomena in master/slave JK Flip Flop.   | 1.                |