University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

Roll No. -

THEORY EXAMINATION – DECEMBER 2018	
B.TECH - ECE	SEMESTER - III

TIME – 3 Hrs.

M.M. - 75

COURSE NO. –ECE-207

COURSE TITLE - DIGITAL ELECTRONICS

Note: All questions in Part-A and Part-B are compulsory. Attempt any four questions from Part-C selecting at least one from each unit.

PART-A (15 Marks)

Q. No. – 1 Answer the following questions. **15x1=15**

(i)	Differentiate between basic gates and universal gates ?
(ii)	Design XNOR gate using only NAND gates.
(iii)	Explain the De-Morgan's theorem with example.
(iv)	Describe Maxterms and Minterms with examples.
(v)	Draw NAND gate using CMOS logic.
(vi)	Which is the fastest Logic Family and why?
(vii)	Differentiate between Latch and Flip-Flop.
(viii)	Describe Programmable Logic Devices and its types.
(ix)	Classify types of Memory? How RAM is different from ROM ?
(x)	What are counters ? what are the various types of Counters ?
(xi)	Describe the truth-table, excitation table, characteristics equation of J-K Flip-Flop.
(xii)	Design a SR flip-flop from T Flip-Flop?
(xiii)	How Asynchronous counters are different from Synchronous counters ?
(xiv)	Differentiate between MUX and DEMUX circuits.
(xv)	Explain how to prevent the indeterminate condition of SR Flip-Flop?

PART-B (20 Marks)

	UNIT-I	
2	Minimize the following SOP equation using four variable K-map and realize The minimized equation using only NAND gates $Z = \Sigma(4,5,6,7,8,9,10,11,12,13,14,15)$	5
	UNIT-II	
3	Differentiate between half adder and full adder. Design a Half Adder using only NAND gates ?	5
	UNIT-III	
4	Write the truth table, excitation table and characteristics equation of SR and JK flip-flops? Draw their logic diagram using gates.	5
	UNIT-IV	
5	Differentiate between PLA and PAL? Implement Full Adder circuit using PLA ?	5

PART-C (40 Marks)

	UNIT-I	
6	Minimize the following SOP equation using four variable K-map and realize The minimized equation using only NAND gates $Z = \Sigma(0,1,2,3,4,8,12)$	10
7	Minimize the following SOP equation using four variable K-map and realize The minimized equation using only NAND gates $Y = \Sigma(9,11,12,13,14,15)$	10
	UNIT-II	
8	Design a 8 to 1 Multiplexer using only NAND gates? How many select lines will be required ? Implement the Full Adder circuit using 8:1 MUX.	10
9	Explain how OR and NOR can be designed in ECL logic family with necessary diagram ?	10
	UNIT-III	
10	What are the various steps involved in designing a synchronous counter? Design a MOD-6 synchronous Counter using T flip-flops.	10
11	Differentiate between combinational and sequential circuits? What are the various types of flip flops? Design T flip flop using D flip-flop.	10
	UNIT-IV	
12	Differentiate between SRAM and DRAM ? Draw the structure and explain the operation of SRAM Cell and DRAM cell.	10
13	Explain the advantages of FPGAs over SPLDs? Explain the structure of CLB and Describe the architecture of FPGA in detail.	10