University Institute of Engineering & Technology

(Recognised Under Section 2(f) and 12B of UGC)

Kurukshetra University, Kurukshetra

Roll No. -

THEORY EXAMINATION – DECEMBER 2016 | **TIME – 3 Hrs.**

B.TECH –ECE | **SEMESTER –3rd** | **M.M. - 75**

COURSE NO. -ECE- 207

COURSE TITLE - Digital Electronics

PART-A (15 Marks)

Q. No. – 1 Answer the following questions carrying one mark each. 15x1=15

(i)	Explain the meaning of negative logic system.
(ii)	Discuss how subtraction is performed by 1's compliment method ?
(iii)	Identify the name of gate which is called any or all gate. Justify the answer.
(iv)	Discuss the basic operations in Boolean algebra.
(v)	What are code converters?
(vi)	List the merits of CMOS logic family ICs.
(vii)	Compare a decoder with a demultiplexer.
(viii)	Interpret the significance of parity bit.
(ix)	How are flip flops different from latches?
(x)	List the various methods used for triggering flip flops.
(xi)	What is meant by modulus of a counter?
(xii)	What does a 32x8 ROM contain?
(xiii)	Define how is the memory size specified?
(xiv)	What is CPLD?
(xv)	Differentiate between PROM and EPROM.

PART-B (20 Marks)

Answer the following questions, all question carrying equal marks. 5x4=20

	UNIT-I	
2	a.)Subtract using 2's compliment method: i)10110 – 1011 ii)1110 – 101110 b.) Describe the procedure of converting Gray number to binary number.	5

	UNIT-II
3	a.)Discuss the working of 4:1 Multiplexer. Explain its logic diagram also. b.)With the help of a neat diagram, explain the working of two- input TTL NAND gate.
	UNIT-III
4	Explain the working of master- slave flip-flop with the help of waveforms. Illustrate the problem encountered inmaster slave flip-flop. How can it be removed?
	UNIT-IV
5	Classify and compare different types of PLDs.

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PART-C (40 Marks)

Attempt four question, by selecting atleast one question from each unit& all question carrying marks. 10x4=40

	UNIT-I
6	Explain Demorgan theorem. How to demorganize an expression? Reduce the following Expressions using Boolean algebra and implement the obtained expression using AOI logic. i) $AB+A(B+C)+B(\overline{B+D})$ ii)$AB+\overline{AC}+A\,\overline{B\,C(AB+C)}$
7	Propose the method of minimization technique using K Map. List the advantages of minimization. Reduce the expression using K-Map and implement it using universal gates. $\prod M(3,6,8,11,13,14).\ d(1,5,7,10)$
	UNIT-II
8	i)How is BCD addition performed? Design a BCD adder to add two 4 bit BCD numbers. ii)Realize the function $F=\sum m(0,1,3,5,8,11,12,14,15)$ using a) 8:1 MUX b) 16:1 MUX
9	List the properties of Logic families. Explain them. Design a two input ECL NAND gate and explain its working.
	UNIT-III
10	i)Design a synchronous sequential circuit having 2 input 2output and is required to produce an output z=1 whenever a sequence 1101 occurs. Overlapping of sequences is allowed. ii)Draw and explain the working of 4-bit parallel in, serial out, shift register.
11	Compare synchronous and asynchronous counters. Design a BCD up/down counter using S-R flip flops.
	UNIT-IV
12	State and explain different types of memories.
13	Implement the following functions using PAL with 4 inputs and 3 wide AND- OR structure. $F1(A,B,C,D)=\sum m(2, 12, 13)$ $F1(A,B,C,D)=\sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$ $F1(A,B,C,D)=\sum m(0, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 15)$ $F1(A,B,C,D)=\sum m(1, 2, 8, 12, 13)$